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In re application of: Mazotti et al.

Attorney Docket No.:

NSC1P271/P05589

Patent: 7,156,562 B2

Issued: January 2, 2007

Title: OPTO-ELECTRONIC MODULE FORM  
FACTOR HAVING ADJUSTABLE OPTICAL  
PLANE HEIGHT

**CERTIFICATE OF MAILING**

I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as first-class mail on July 19, 2007 in an envelope addressed to the Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450.

Signed: \_\_\_\_\_

Aurelia M. Sanchez

**REQUEST FOR CERTIFICATE OF CORRECTION  
OF OFFICE MISTAKE  
(35 U.S.C. §254, 37 CFR §1.322)**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450  
Attn: Certificate of Correction

**Certificate**  
**JUL 25 2007**  
**of Correction**

Dear Sir:

Attached is Form PTO-1050 (Certificate of Correction) at least one copy of which is suitable for printing. The errors together with the exact page and line number where the errors are shown correctly in the application file are as follows:

**SPECIFICATION:**

1. Column 7, line 30, change "tat allow" to --that allow--. This appears correctly in the patent application as filed on July 15, 2003, on page 10, line 26.

**CLAIMS:**

1. In line 39 of claim 1 (column 11, line 62) change "ease" to --case--. This appears correctly in Amendment E as filed on September 21, 2006, on page 3, paragraph 1, line 1.

2. In line 1 of claim 5 (column 12, line 23) change "Art" to --An--. This appears correctly in Amendment E as filed on September 21, 2006, on page 3, paragraph 5, line 1.

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3. In line 5 of claim 5 (column 12, line 27) change "flex tape" to --flexi tape--. This appears correctly in Amendment E as filed on September 21, 2006, on page 3, paragraph 5, line 3.

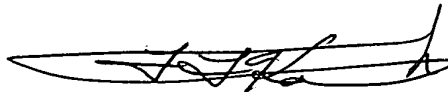
4. In line 5 of claim 26 (column 14, line 9) change "ease" to --case--. This appears correctly in Amendment E as filed on September 21, 2006, on page 7, paragraph 2, line 3.

5. In line 28 of claim 27 (column 14, line 40) change "part end" to --port end--. This appears correctly in Amendment E as filed on September 21, 2006, on page 8, paragraph 1, line 4.

Patentee hereby requests expedited issuance of the Certificate of Correction because the error lies with the Office and because the error is clearly disclosed in the records of the Office. As required for expedited issuance, enclosed is documentation that unequivocally supports the patentee's assertion without needing reference to the patent file wrapper.

It is noted that the above-identified errors were printing errors that apparently occurred during the printing process. Accordingly, it is believed that no fees are due in connection with the filing of this Request for Certificate of Correction. However, if it is determined that any fees are due, the Commissioner is hereby authorized to charge such fees to Deposit Account 500388 (Order No. NSC1P271).

Respectfully submitted,  
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Electrical interface substrate 206 can also support various electrical components 212. However, in some embodiments, substrate 206 does not support electrical components 212 and functions mainly to support circuitry that connects one end of the substrate to the other. Specifically, such circuitry connects electrical contacts 218, which formed electrical port 214. Electrical contacts 218 can be formed on the top and/or bottom surfaces of electrical interface substrate 206. The dimensions of substrate 206 should be such that they allow system 200 to fit within certain standard requirements.

OE support substrate 204 and substrate 206 have circuitry that is embedded or on a top and/or bottom surface of substrate 204. Such circuitry is used to interconnect the various components mounted onto either the top or bottom surfaces of the substrate. In one common embodiment, substrates 204 and 206 are resin-based printed circuit boards. Substrates 204 and 206 are typically substantially rigid. Such rigidity allows for certain components and ports to be positioned in certain orientations with a degree of certainty.

OE device 210 generally includes one or more photonic devices that are directly or indirectly connected to a semiconductor device. As discussed above, the photonic device functions to send and receive optical data signals and the semiconductor device acts to convert the optical signals from the photonic devices into electrical signals and vice-versa. The height at which the photonics are located typically determines the optical plane height, unless various mirrors and/or lenses alter the height.

OE device 210 as shown in FIG. 4 includes a semiconductor chip package 220, a support block 222, and a barrel unit 224. It is not shown in FIGS. 4 or 5, but at least one photonic device is attached to support block 222. See FIG. 6 for one embodiment of an OE device 300 wherein the photonic devices 302 are shown. Semiconductor chip package 220 is any type of package having a semiconductor chip that is at least partially encapsulated within a protective material, such as epoxy or resin. Chip package 200 should have electrical traces and/or contacts that allow for electrical connection with support block 222. In one embodiment, a semiconductor die within the chip package will have uplinking electrical contacts formed directly on the top surface of the die. These uplinking contacts are exposed through the top surface of the chip package 220 and thereby can be connected to contact pads of support block 222. Traces on the surface or within support block 222 serve to connect chip package 220 to the photonic devices attached to support block 222. In FIGS. 4 and 5, the photonic devices are attached to the front face of support block 222, which is the face to which barrel unit 224 is attached. The hollow barrels 226 provide access for an optical connection to

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an external case configured to enclose the first and second substrates as well as all components mounted thereon, the case enabling optical communication between the optical device package and an external optical component and enabling electrical connection to the port end of the second substrate.

**2. (Previously Presented):** An opto-electronic module as recited in claim 1 wherein the conductive lines of the flex connector are suitable for transmitting differential signals between the first and the second substrate.

**3. (Previously Presented):** An opto-electronic module as recited in claim 2 wherein the conductive lines of the flex connector are connected to the interior end of the second substrate and the interior end of the first substrate.

**4. (Previously Presented):** An opto-electronic module as recited in claim 1 wherein the semiconductor chip package includes:

a semiconductor die that is at least partially encapsulated within a protective molding material;

wherein the top electrical contacts of the chip package comprise electrical contacts formed on a top surface of the semiconductor die such that that the contacts are exposed through a surface of the protective molding material; and

wherein the optical device package is mounted to the top surface of the protective molding material such that the optical device package is electrically connected to the chip package using the electrical traces of the support block and the exposed electrical contacts.

**5. (Previously Presented):** An opto-electronic module as recited in claim 4 wherein the optical device package is suitable for receiving or sending optical signals; and

wherein the support block includes electrical traces formed on a flexi tape that is mounted on the support block and extends from the first face to the second face of the block so that the optical device package is electrically connected to the electrical traces of the flexi tape and the exposed electrical contacts of the semiconductor package.

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external case is further configured to secure the substrates at two different heights defined by the electro-optic form factor for which the module is to be employed.

**34. (Previously Presented):** An opto-electronic module as recited in claim 32 wherein the first substrate is mounted to the bottom interior surface of the external case and the second substrate is elevated above the bottom interior surface of the external case and not in contact with an upper interior surface of the external case.

**35. (Previously Presented):** An opto-electronic module as recited in claim 21 wherein the integrally formed flex connector comprises a thinned substrate integrally formed as part of the first and the second substrate.

**36. (Cancelled).**

**37. (Previously Presented):** An opto-electronic module having an optical port and an electrical port comprising:

- a first planar substrate having electrical traces, an optical port end, and an opposite interior end;

- an opto-electronic device attached to and electrically connected to the first substrate at the optical port end, wherein the opto-electronic device serves as the optical port wherein the opto-electronic device comprises:

- a semiconductor chip package having upper chip electrical contacts on a top surface of the package and having lower chip electrical contacts on a lower surface of the package, the package being mounted directly on top of the first substrate;

- a support block having a first face and a second face that are angled relative to one another with electrical traces that extend from the first face to the second face wherein the first face of the support block is mounted on top of the chip package so that at least some of the upper chip electrical contacts are electrically coupled to associated traces on the first face of the support block; and

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a optical device package mounted on the second face of the support block, the optical device package having at least one active facet thereon and having electrical contacts that are electrically coupled to associated traces on the support block;

a second planar substrate having electrical traces, the second substrate having a port end on an end opposite from an interior end, wherein the port end forms the electrical port for electrically connecting the opto-electronic module with an external electrical device; and

an intermediate substrate of a predetermined offset thickness containing a plurality of electrically conductive lines, wherein the plurality of electrically conductive lines of the intermediate substrate connect the electrical traces of the first and the second substrates, wherein the thickness of the intermediate substrate separates the height of the optical port with respect to the height of the electrical port by a desired offset distance.

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(Also Form PT-1050)

**UNITED STATES PATENT AND TRADEMARK OFFICE  
CERTIFICATE OF CORRECTION**

PATENT NO. : 7,156,562 B2

Page 1 of 1

DATED : January 2, 2007

INVENTOR(S) : Mazotti et al.

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

**In the Specification:**

Column 7, line 30, change "tat allow" to --that allow--.

**In the Claims:**

In line 39 of claim 1 (column 11, line 62) change "ease" to --case--.

In line 1 of claim 5 (column 12, line 23) change "Art" to --An--.

In line 5 of claim 5 (column 12, line 27) change "flex tape" to --flexi tape--.

In line 5 of claim 26 (column 14, line 9) change "ease" to --case--.

In line 28 of claim 27 (column 14, line 40) change "part end" to --port end--.

MAILING ADDRESS OF SENDER:

PATENT NO. 7,156,562 B2

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